4. (amended) A method according to claim 1 wherein the operation of storage of a register involves a mix of multiplication, division, or shift operations.

5. (amended) A method according to claim 1 wherein the entire operation of the method or parts of the method are embodied within digital logic gates.

6. (amended) A method according to claim 1 wherein the entire operations of the method or parts of the method are embodied within a Hamiltonian or other matrix operation.

7. (amended) A method according to claim 1 wherein all values to be incorporated into the resulting EPC code are extracted from input and from the UPC code before being incorporated, via a single bit-field storage command into the target EPC storage range.

REMARKS - General

By the above amendment, Applicant has amended the specification to correct the formatting imposed by the U.S.P.T.O's discontinued PASAT EFS system to the code listing. In particular, the end-of-line characters have been reintroduced to render the code more readable. No substantive changes are requested.

By the above amendment, Applicant has amended the claims to resolve claim objection 1: The formatting imposed by the U.S.P.T.O's discontinued PASAT EFS system of square brackets about claim numbers has been changed as requested by Examiner to simple numbers of the format 1., 2., etc.

By the above amendment, Applicant has amended the claims to address the second and third issues of Examiner's claim objection 1 – replacing, "it" with – "the method".

The Claims Rejections on the Basis of Bauer et al and Omekchenko, Under § 103

The O.A. rejected independent claim 1 and dependent claims 2-5 on Bauer et al in view of Omelchenko, essentially stating that "it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to further employ an increased operational speed of BCD into binary-code conversion in addition to the conversion method of a UPC format to an EPC format of Bauer et al. due to the fact that faster conversion can be accomplished by simultaneously adding of lower and higher digits.

Applicant requests reconsideration and withdrawal of this rejection on the following basis. It is well known that in order for any prior-art references themselves to be validly combined for use in a §103

rejection, the references themselves (or some other prior art) must suggest that they be combined. E.g. as was stated in In re Sernaker, 217 U.S.P.Q. 1, 6 (C.A.F.C. 1983):

> "[P]rior art references in combination do not make an invention obvious unless something in the prior art references would suggest the advantage to be derived from combining their teachings."

From the Board statement in Ex parte Levengood, 28 U.S.P.Q.2d 1300 (P.T.O.B.A&I. 1993):

> "Our reviewing courts have often advised the Patent and Trademark Office that it can satisfy the burden of establishing a prima facie case of obviousness only by showing some objective teaching in either the prior art, or knowledge generally available to one of ordinary skill in the art, that 'would lead' that individual 'to combine the relevant teachings of the references.' Accordingly, an examiner cannot establish obviousness by locating references which describe various aspects of a patent applicant's invention without also providing evidence of the motivating force which would impel one skilled in the art to do what the patent applicant has done."

In the present case, the reason given in the O.A. describes the "increased operational speed of BCD into binary-code conversion." Bauer et al., however, do not reference Omelchenko. As stated in the O.A., "Bauer et al. are silent about the claimed means of loading and storing registers and the means of multiplying, dividing, shifting or adding register contents." Bauer et al. do not describe using shift operations to obtain a conversion. **Bauer et. al. do not refer to any BCD conversion operation at all, merely to "converting to a binary representation."** Such a conversion may sound deceptively similar but it is specifically not BCD conversion. For example, BCD encoding of decimal 90 is the sixteen bit 0x0900, while a compact binary representation of the same value is 0x005a. As will be explained later, this prevents the application of BCD and Omelchenko to Bauer et. al for the purpose of UPC to EPC conversion.

Even if Bauer et al. and Omelchenko Were to be Combined in the Manner Proposed, the Proposed Combination Would Not Show the Advantage of Claim 1. Claim 1 has novel and non-obvious advantages over the proposed combination. Specifically, binary coded decimal is a code format that is ***explicitly not used*** in EPC coding because of its loss in efficiency. The 96 bits of the EPC format are intended to be sufficient for numbering every object ever tagged. The goal of the EPC format is efficiency, and, in fact, the format is designed for efficiency. Therefore, conventional wisdom and teaching is that an inefficiency of the sort introduced by BCD coding is to be avoided.

The specification presents multiple step-by-step methods for performing actual conversion between UPC and EPC formats that are not described or contemplated in Bauer et. al or Omelchenko. Thus the Applicant respectfully submits that the methods described in the specification and the resulting claims are unique and distinct from the prior art of Bauer et al., and Omelchenko.

The O.A. rejected claim 6 on Bauer et al in view of Omelchenko and Avgul, stating that "it would have been obvious at the time the invention was made to a person of ordinary skill in the art to have incorporated the matrix operations calculator as taught by Avgul into the teachings of Bauer et al. in view of Omelchenko for the purpose of maximizing productivity within the step of operations involved with various logic gates."

As mentioned above, the use of BCD in the conversion from UPC to EPC is counter-intuitive. Conventional wisdom teaches against using an inherently inefficient representation such as BCD when converting to a format such as the EPC that is designed for efficiency. As such, the underlying combination of Bauer et al. and Omelchenko is non-obvious, therefore rendering the addition of Avgul non-obvious. In addition, although Avgul teaches the use of a matrix operations calculator, no mention is made of the benefit of using such a matrix to increase speed or efficiency in the conversion of UPC to EPC formats or in the use of conversion to BCD.

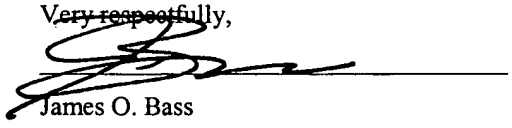
Applicant respectfully notes that although Claim 7 was listed as rejected, no reason was explicitly given as was the case with Claims 1-6.

Applicant respectfully requests, if the claims are again rejected upon any combination of references that the rejecting O.A. include an explanation, in accordance with M.P.E.P. § 706.02, Ex parte Clapp, 27 U.S.P.Q. 972 (P.O.B.A. 1985) and Ex parte Levengood, supra, a "factual basis to support the conclusion that it would have been obvious," to make the combination.

CONCLUSION

For the reasons given above, applicant respectfully submits that the specification and claims have been amended per request in the O.A., the claims are distinct and of patentable merit under Section 103 because of the counter-intuitive use of BCD in the conversion from UPC to EPC as explained above. Accordingly, applicant submits that this application is now in full condition for allowance, which action applicant respectfully solicits.

Very respectfully,



James O. Bass

Attorney, Reg # 53974

Appendix A: Claim Markups.

[c1]1. A method [and apparatus] for converting or translating descriptions of products encoded in the Universal Product Code (UPC) or Uniform Code Council 12 (UCC-12) format to the Electronic Product Code (EPC) format comprising: -

-a means of loading and storing registers; -

-and a means of multiplying, dividing, shifting or adding register contents. --

[c2]2. A method according to claim 1 wherein the operation of storage of a register involves only shift operations. --

[c3]3. A method according to claim 1 wherein the operation of storage of a register involves only multiplication or division operations. --

[c4]4. A method according to claim 1 wherein the operation of storage of a register involves a mix of multiplication, division, or shift operations. --

[c5]5. A method according to claim 1 wherein the entire operation of the method or parts of [it] the method are embodied within digital logic gates. --

[c6]6. A method according to claim 1 wherein the entire operations of the method or parts of [it] the method are embodied within a Hamiltonian or other matrix operation. --

[c7]7. A method according to claim 1 wherein all values to be incorporated into the resulting EPC code are extracted from input and from the UPC code before being incorporated, via a single bit-field storage command into the target EPC storage range. ---

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May 24, 2005

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re:	Application Number	:	10/707,216
	Applicant	:	Nick Hilliard
	Filed	:	11/26/2003
	Title	:	Universal product code conversion to electronic product code
	Examiner	:	S. Paik

Sir:

Please find attached a response to the Office Action mailed 02/24/2005.

Respectfully,

James O. Bass
Reg # 53974